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| 08/602,503 | 02/20/1996 | MICHAEL B. BALL | 2718US | 4539 |

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| EXAMINER | |
|---|---|
| NGUYEN, DILINH P | |
| **ART UNIT** | **PAPER NUMBER** |
| 2814 | |

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 08/602,503 | BALL, MICHAEL B. | |
| | Examiner | Art Unit | |
| | DiLinh Nguyen | 2814 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *19,21-23 and 25-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19,21-23,25,27,29-34* is/are rejected.

7)☒ Claim(s) *26 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yasuhide et al. (J.P. 63-179537) in view of Minahan et al. (U.S. Pat. 5279991) and further in view of Kaiser (U.S. Pat. 5281846).

Yasuhide et al. disclose a method of fabricating a multi-die assembly, comprising:

providing a substrate 4 including a plurality of conductors 4-1;

attaching at least one active face down base die 1 to the substrate in electrical communication with at least some of the plurality of conductors 4-1;

providing a layer of adhesive 1-1 to a back side of the at least one base die;

placing a back side of at least one active face up stack die 2 on the layer of adhesive 1-1;

securing the back side of at least one stack die to the at least one base die (fig. 1c).

Yasuhide et al. do not explicitly disclose the step of curing the adhesive wherein the adhesive layer is an electrically conductive epoxy adhesive and providing a direct electrical path between the dice.

However, Minahan et al. disclose a method of fabricating a multi-die assembly, comprising the step of curing the adhesive layer between adjacent chips (abstract and column 3, lines 13-19) for the purpose of making high density electronics and assure in reliability for the semiconductor package (abstract).

Kaiser discloses a method of fabricating a multi-die assembly, comprising:

providing a base die 14;

providing a back side of at least one active face up stack die 22 on the layer of electrically conductive epoxy adhesive 20 and securing the back side of at least one stack die to the at one base die (fig. 1);

providing the electrically conductive adhesive 20 (fig. 1, column 2, lines 55-56) is between the base die and the stack die;

providing a direct electrical path between the at least one stack die and base die (column 2, lines 27-32);

electrically grounding the at least one base die via the layer of electrically conductive adhesive and the at least one stack die (fig. 1) in order to provide an electrical connection between the chips (fig. 1).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the process step of Yasuhide et al. by curing the adhesive layer between adjacent chips and forming the electrically conductive adhesive between the base die and the active face up stack die, as taught by Minahan et al. and Kaiser, for the purpose of making high density electronics, assure in reliability and in order to provide an electrical connection between the chips.

3. Claims 21-23, 25, 27, 29 and 33-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasuhide et al. (J.P. 63-179537) and Minahan et al. (U.S. Pat. 5279991) in view of Kaiser (U.S. Pat. 5281846) and further in view of Fogal et al. (U.S. Pat. 5323060).

Yasuhide et al., Minahan et al. and Kaiser fail to disclose at least one discrete component to at least one of the stack die, the base die or the substrate.

Fogal et al. disclose a multichip module (fig. 5, column 3, lines 43 et seq.) comprising:

a discrete component 75 to the substrate 12;

a discrete components 76 and 78 to an adhesive layer 77 to an upper uppermost chip 85; and

a bond wires 44a, 44b, and 79-81, wherein the bond wires bonding to the substrate and the chips. Fogal et al. show that discrete components can be added, while it is not specifically pointed out, the discrete component could include a filer (by pass) capacitor (column 3, line 53) which is needed for proper device operation and is not normally formed as part of a chip. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the process step of the above combination by having at least one discrete component to at least one of the stack die, the base die or the substrate, as taught by Fogal et al., to provide additional necessary components.

- Regarding claim 22, Fogal et al. disclose extending a component to substrate bond wire 79/44b between the at least one discrete component 76/75 and at least one of the plurality of substrate conductors (fig. 5).
- Regarding claim 23, Fogal et al. disclose a multi-chip semiconductor (fig. 1, column 2, lines 35 et seq.) comprising: securing at least another stack die 54 to the assembly and electrically connecting the at least another stack die and at least one of the plurality of substrate conductors.
- Regarding claim 25, Fogal et al. disclose securing the at least another stack die 54 to the at least one stack die 28.
- Regarding claim 27, Fogal et al. disclose securing at least one discrete component 76/78 to at least one stack die and extending a component to substrate bond wire 79 between the at least one discrete component and at least one of the plurality of substrate conductors.
- Regarding claim 29, Fogal et al. disclose securing at least one discrete component to the at least one base die, and extending a component to substrate bond wire 79/44b between the at least one discrete component and at least one of the plurality of substrate conductors.
- Regarding claim 33, Fogal et al. disclose securing at least one discrete component to the substrate; and extending a die to component bond wire between the at least one stack die and the at least one discrete component.

- Regarding claim 34, Fogal et al. disclose extending a die to component bond wire 79/44b between the at least one discrete component and at least one of the plurality of substrate conductors.

4. Claims 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasuhide et al. (J.P. 63-179537) and Minahan et al. (U.S. Pat. 5279991) in view of Kaiser (U.S. Pat. 5281846) and further in view of Rostoker (U.S. Pat. 5399898).

Yasuhide et al., Minahan et al. and Kaiser disclose the claimed invention except for not further disclose the face down base die includes attaching at least two active face down base die to the substrate.

Rostoker discloses the attaching at least one active face down base die includes attaching at least two active face down base die 404 and 410 (fig. 4a, column 14, lines 40 et seq.) to the substrate 402 and electrically coupling each of the base die with one of the plurality substrate conductors 406 and 412; a bridging 416 at least one stack die between the two base die; and further comprising securing at least another stack die over the at least one stack die (fig. 3b). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the process step of the above combination by having the step of attaching at least two active face down base die to the substrate, as taught by Rostoker, to provide a greater power dissipation and a natural convection cooling channel and design flexibility in mounting semiconductor devices.

***Allowable Subject Matter***

Claims 26 and 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance:

The prior art of record fail to disclose the combination of all the limitations recited, including securing at least one discrete component to the at least one stack die; and extending a die to component bond wire between the at least another stack die and the at least one discrete component and securing at least one discrete component to the at least one base die; and extending a die to component bond wire between the at least another stack die and the at least one discrete component.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Response to Arguments***

Applicant's arguments filed 9/30/05 have been fully considered but they are not persuasive.

- The applicant argues that Yasuhide et al. does not teach how either of the semiconductor devices are electrically grounded, and does not teach or suggest grounding the first semiconductor device through the second conductor device by way

of electrically conductive epoxy adhesive provided between the first semiconductor device and the second semiconductor device.

The arguments have been fully considered but they are not persuasive because this argument has no immediate apparent relevance to the issues presented by the rejection before us since an appellant cannot show nonobviousness by attacking references individually wherein the rejection is based upon a combination of references. In re Young, 403 F. 2d 754,757,159 USPQ 725, 728 (CCPA 1968).

It should be noted that the rejection of claim 19 is not based on anticipation, but rather, is based on obviousness.

Examiner relies on the combined teachings at Yasuhide et al. and Kaiser. Yasuhide et al. is not relied on for teaching the electrically conductive epoxy adhesive; providing a direct electrical path between the at least one stack die and at least one of the plurality of conductors; and electrically grounding the at least one base die via the layer of electrically conductive epoxy adhesive.

Yasuhide et al. is relied on for showing a substrate 4 including a plurality of conductors 4-1; attaching at least one active face down base die 1 to the substrate in electrical communication with at least some of the plurality of conductors 4-1; placing a back side of at least one active face up stack die 2; securing the back side of at least one stack die to the at least one base die (fig. 1c). The examiner thus regards the applicant's assertions as constituting evidence that the applicant has failed to consider as a whole the prior art teachings disclosed by the combining of the references.

- In response to applicant's argument that there is no motivation to combine the

references, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

- The applicant argues that Minahan et al. does not teach electrically conductive adhesive. Further, Minahan et al. does not teach how the semiconductor devices described therein are electrically grounded, and does not teach or suggest grounding a base semiconductor device through another semiconductor device that is mounted thereon by way of electrically conductive epoxy adhesive between the base semiconductor device and the semiconductor device mounted thereon.

The arguments have been fully considered but they are not persuasive because this argument has no immediate apparent relevance to the issues presented by the rejection before us since an appellant cannot show nonobviousness by attacking references individually wherein the rejection is based upon a combination of references. In re Young, 403 F. 2d 754,757,159 USPQ 725, 728 (CCPA 1968).

It should be noted that the rejection of claim 19 is not based on anticipation, but rather, is based on obviousness.

Examiner relies on the combined teachings at Yasuhide et al. in view Minahan et al. and further in view of Kaiser. Minahan et al. is relied on for curing the adhesive layer between adjacent chips (abstract and column 3, lines 13-19) for the

purpose of making high density electronics and assure in reliability for the semiconductor package (abstract). The examiner thus regards the applicant's assertions as constituting evidence that the applicant has failed to consider as a whole the prior art teachings disclosed by the combining of the references.

- The applicant argues that Kaiser does not teach how the semiconductor chip described therein is electrically grounded, and does not teach or suggest grounding the semiconductor chip through another semiconductor chip that is mounted thereon by way of electrically conductive adhesive.

The arguments have been fully considered but they are not persuasive because Kaiser clearly disclose providing a base die (capacitor) 14; providing a back side of at least one active face up stack die 22 on the layer of electrically conductive epoxy adhesive 20 (fig. 1); providing the electrically conductive adhesive 20 (fig. 1, column 2, lines 55-56) is between the base die and the stack die; providing a direct electrical path between the at least one stack die and base die (column 2, lines 27-32); electrically grounding the at least one base die via the layer of electrically conductive adhesive and the at least one stack die (fig. 1).

The semiconductor chip could be a passive electronic component, wherein the electronic component may be a resistor, a diode, a decoupling capacitor, or the like. Therefore, the capacitor of Kaiser is a semiconductor chip or base die 14 to the substrate.

Kaiser clearly discloses a semiconductor package comprising: a substrate, a base die; a electrically conductive epoxy adhesive 20; a stack die 22; providing a direct

electrical path between the at least one stack die and at least one stack die. It should be noted that: for performing the electrical functions, the circuitry of the Kaiser's package capable of grounding the base die 14 via the layer of electrically conductive epoxy adhesive 20 and the at least one stack die 22 (fig. 1).

***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DiLinh Nguyen whose telephone number is (571) 272-1712. The examiner can normally be reached on 8:00AM - 6:00PM (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DLN

HOAI PHAM
PRIMARY EXAMINER